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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/572,725	03/21/2006	Seon Ho Han	CU-4700 WWP	6890

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EXAMINER
HSIEH, PING Y

ART UNIT	PAPER NUMBER
2618	

MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/572,725	HAN ET AL.	
	Examiner	Art Unit	
	PING Y. HSIEH	2618	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 February 2010*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,8 and 21-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,8,22,24 and 26* is/are rejected.

7)☒ Claim(s) *21,23 and 25* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 February 2010* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Drawings

The drawings were received on 2/12/10. These drawings are acceptable.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 3 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al. (U.S. PG-PUB NO. 2004/0048591) in view of Welland et al. (U.S. PG-PUB NO. 2003/0119467).

-Regarding claims 1, 3 and 8, Kim discloses an RF front-end transceiver comprising:

a frequency synthesizer or a base band processor for providing a frequency control voltage signal **(frequency synthesizer as disclosed in paragraph 47)**;

an oscillator for outputting a resonant frequency signal such that a frequency of the resonant frequency signal is controlled by the frequency control voltage signal **(VCO as shown in fig. 2)**;

a receive amplifier for amplifying and outputting a receive RF signal **(low noise amplifier 240 as disclosed in fig. 2 and further disclosed in paragraph 42)**;

a receive mixer for mixing the receive RF signal amplified and the resonant frequency signal to convert the receive RF signal into a receive base band signal **(down mixer 211 as disclosed in fig. 2)**;

a transmit mixer for mixing a transmit base band signal and the resonant frequency signal to convert the transmit base band signal into a transmit RF signal **(up mixer 214 as disclosed in fig. 2)**; and

a transmit amplifier for amplifying and outputting the transmit RF signal **(power amplifier 280 as disclosed in fig. 2)**,

wherein at least one of the receive amplifier, the receive mixer, the transmit mixer and the transmit amplifier includes a resonant unit, the resonant unit being controlled by only the frequency control voltage signal **(as shown in fig. 1A and 1B)**.

However, Kim fails to specifically disclose the frequency control voltage signal including a digital frequency control voltage (VDT) signal and an analog frequency control voltage (VAT) signal.

Welland et al. disclose the oscillator is a digital analog tuning voltage controlled oscillator for providing the output resonant frequency, f_{LO} **(VCO 400 is a digital analog VCO as disclosed in fig. 5 and further disclosed in**

paragraph 56-60); and VCO is controlled by VAT and VDT signals **(Vc and Bc signals as disclosed in fig. 5)**.

Therefore, it would have been obvious to one of ordinary skills in the art at the time of invention to modify the PLL of Kim to include the frequency synthesizer as disclosed by Welland et al. One is motivated as such in order to integrate the VCO with the other components of the PLL onto a single integrated circuit for size consideration.

-Regarding claims 22, 24 and 26, the combination further discloses each of the receive amplifier **(Kim, fig. 5)**, the receive mixer **(Kim, fig. 7)**, the transmit mixer **(Kim, fig. 7)** and the transmit amplifier **(Kim, fig. 6)** includes the resonant unit.

Allowable Subject Matter

Claims 21, 23 and 25 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

Applicant's arguments filed 2/12/10 have been fully considered but they are not persuasive.

a. In pages 6-10 of the remarks, regarding claims 1, 3 and 8, applicant argues that Kim discloses only control voltage which is an analog signal is used to control a LNA and a down mixer; and Welland does not disclose the control

voltage from the frequency synthesizer is used to control the receive amplifier or the receive mixer. Applicant further argues that the present invention has unexpected advantages and it is not obvious to modify the PLL of Kim to include the frequency synthesizer as disclosed by Welland.

-The examiner respectfully disagrees. In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Even thought Kim fails to specifically disclose the frequency control voltage signal including a digital frequency control voltage (VDT) signal and an analog frequency control voltage (VAT) signal, Welland et al. disclose the oscillator is a digital analog tuning voltage controlled oscillator for providing the output resonant frequency, f_{LO} **(VCO 400 is a digital analog VCO as disclosed in fig. 5 and further disclosed in paragraph 56-60)**; and VCO is controlled by VAT and VDT signals **(Vc and Bc signals as disclosed in fig. 5)**. Therefore, it would have been obvious to one of ordinary skills in the art at the time of invention to modify the PLL of Kim to include the frequency synthesizer as disclosed by Welland et al. One is motivated as such in order to integrate the VCO with the other components of the PLL onto a single integrated circuit for size consideration.

Welland further discloses implementing a phase-locked loop (PLL) frequency synthesizer with a variable capacitance voltage controlled oscillator (VCO) that includes a discretely variable capacitance in conjunction with a continuously variable capacitance is advantageous since the discretely variable capacitance may provide coarse tuning adjustment of the variable capacitance to compensate for capacitor and inductor tolerances and to adjust the output frequency to be near the desired output frequency; and the continuously variable capacitance may provide a fine tuning adjustment of the variable capacitance to focus the output frequency to match precisely the desired output frequency and to provide compensation for post-calibration drift of the PLL circuitry **(see Welland, paragraph 11)**. Therefore, the result of the combination is expected.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to PING Y. HSIEH whose telephone number is (571)270-3011. The examiner can normally be reached on Monday~Thursday 8am ~ 4pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nay Maung can be reached on 571-272-7882. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/P. Y. H./
Examiner, Art Unit 2618

/Lana N. Le/
Primary Examiner, Art Unit 2614